

## CLAIMS

What is claimed is:

1           1.       A microelectronic device, comprising:  
2           a microelectronic die having an active surface, a back surface, and at least one  
3           side;  
4           said at least one microelectronic die side comprising at least one trench sidewall,  
5           at least one lip and at least one channel sidewall; and  
6           a metallization layer disposed on said microelectronic die back surface and said at  
7           least one trench sidewall.

1           2.       The microelectronic device of claim 1, wherein said at least one trench  
2           sidewall is substantially planar to said at least one channel sidewall.

1           3.       The microelectronic device of claim 2, wherein said at least one lip is  
2           substantially perpendicular to at least one of said at least one trench sidewall and at least  
3           one channel sidewall.

1           4.       The microelectronic device of claim 2, wherein said at least one lip is  
2           substantially angled to at least one of said at least one trench sidewall and at least one  
3           channel sidewall.

1           5.       The microelectronic device of claim 2, wherein said at least one lip is  
2 substantially curved to at least one of said at least one trench sidewall and at least one  
3 channel sidewall.

1           6.       The microelectronic device of claim 1, wherein said metallization layer is  
2 at least one metal selected from the group consisting of gold, silver, titanium, chromium,  
3 vanadium, tungsten, and nickel.

1           7.       A microelectronic device assembly, comprising:  
2 a microelectronic die having an active surface, a back surface, and at least one  
3 side;  
4 said at least one microelectronic die side comprising at least one trench sidewall,  
5 at least one lip, and at least one channel sidewall;  
6 a metallization layer disposed on said microelectronic die back surface and said at  
7 least one trench sidewall; and  
8 a heat dissipation device attached to said microelectronic die back surface with a  
9 thermal interface material.

1           8.       The microelectronic device assembly of claim 7, wherein said at least one  
2 trench sidewall is substantially planar to said at least one channel sidewall.

1           9.     The microelectronic device assembly of claim 8, wherein said at least one  
2 lip is substantially perpendicular to at least one of said at least one trench sidewall and at  
3 least one channel sidewall.

1           10.    The microelectronic device of claim 8, wherein said at least one lip is  
2 substantially angled to at least one of said at least one trench sidewall and at least one  
3 channel sidewall.

1           11.    The microelectronic device of claim 8, wherein said at least one lip is  
2 substantially curved to at least one of said at least one trench sidewall and at least one  
3 channel sidewall.

1           12.    The microelectronic device assembly of claim 7, wherein said  
2 metallization layer is at least one metal selected from the group consisting of gold, silver,  
3 titanium, chromium, vanadium, tungsten, and nickel.

1           13.    The microelectronic device assembly of claim 7, wherein said thermal  
2 interface material is selected from the group consisting of lead, tin, indium, silver,  
3 copper, and alloys thereof.

1           14.     The microelectronic device assembly of claim 7, wherein at least a portion  
2     of a fillet of said thermal interface material extend from said metallization layer on said  
3     microelectronic die trench sidewall to said heat dissipation device.

1           15.     A method of dicing a microelectronic device wafer, comprising:  
2           providing a microelectronic device wafer comprising a semiconductor wafer  
3     having a back surface, said microelectronic device including at least two integrated  
4     circuit areas formed therein separated by at least one scribe street;  
5           forming at least one trench opposing said at least one scribe street and extending  
6     from said semiconductor wafer back surface into said semiconductor wafer, wherein said  
7     trench comprises at least two sidewalls and a bottom portion;  
8           forming a metallization layer on said semiconductor wafer back surface, said at  
9     least two trench sidewalls and said trench bottom portion; and  
10          forming a channel within said at least one scribe street and extending through said  
11     interconnection layer, said semiconductor wafer, and said metallization layer in said  
12     trench bottom portion.

1           16.     The method of claim 15, wherein providing said microelectronic further  
2     includes providing said microelectronic device wafer having an interconnection layer  
3     disposed on said active surface.

1           17.     The method of claim 15, wherein forming said trench comprises forming  
2     at least one trench that is wider than said channel.

1           18.     The method of claim 15, wherein forming said trench comprises forming  
2     said trench by a method selected from the group consisting of laser ablation, wet etching,  
3     dry etching, reactive ion etching, and cutting with a wafer saw.

1           19.     The method of claim 15, wherein forming said metallization layer  
2     comprises depositing a layer of metal selected from the group consisting of gold, silver,  
3     titanium, chromium, vanadium, tungsten, and nickel.

1           20.     A method of fabricating a microelectronic device assembly, comprising:  
2             providing a microelectronic die having an active surface, a back surface, and at  
3     least one side, wherein said at least one microelectronic die side comprises at least one  
4     trench sidewall, at least one lip and at least one channel sidewall;  
5             disposing a metallization layer on said microelectronic die back surface and said  
6     at least one trench sidewall; and  
7             attaching a heat dissipation device to said microelectronic die back surface with a  
8     thermal interface material.

1           21.     The method of claim 20, wherein disposing said metallization layer  
2 comprises disposing a metal selected from the group consisting of gold, silver, titanium,  
3 chromium, vanadium, tungsten, and nickel on said microelectronic die back surface.

1           22.     The method of claim 20, wherein attaching said heat dissipation device  
2 comprises attaching said heat dissipation device with a thermal interface material selected  
3 from the group consisting of lead, tin, indium, silver, copper, and alloys thereof.

1           23.     The method of claim 20, wherein attaching said heat dissipation device  
2 comprises attaching said heat dissipation device with said thermal interface material such  
3 that a portion of a fillet of said thermal interface material extends from said metallization  
4 layer on said trench sidewall to said heat dissipation device.

1           24.     The method of claim 20, wherein providing said microelectronic die  
2 comprises:  
3           providing a microelectronic device wafer comprising a semiconductor wafer  
4 having a back surface, said microelectronic device including at least two integrated  
5 circuit areas formed therein separated by at least one scribe street;  
6           forming at least one trench opposing said at least one scribe street and extending  
7 from said semiconductor wafer back surface into said semiconductor wafer, wherein said  
8 trench comprises at least two sidewalls and a bottom portion;

9 forming a metallization layer on said semiconductor wafer back surface, said at  
10 least two trench sidewalls and said trench bottom portion; and  
11 forming a channel within said at least one scribe street and extending through said  
12 interconnection layer, said semiconductor wafer, and said metallization layer in said  
13 trench bottom portion.

1 25. The method of claim 24, wherein providing said microelectronic die  
2 further includes providing said microelectronic device wafer having an interconnection  
3 layer disposed on said active surface.

1 26. The method of claim 24, wherein forming said trench comprising forming  
2 at least one trench which is wider than said channel.

1 27. The method of claim 24, wherein forming said trench comprises forming  
2 said trench by a method selected from the group consisting of laser ablation, wet etching,  
3 dry etching, reactive ion etching, and cutting with a wafer saw.

1 28. The method of claim 24, wherein forming said metallization layer  
2 comprises depositing a layer of metal selected from the group consisting of gold, silver,  
3 titanium, chromium, vanadium, tungsten, and nickel.